Product Summary

Single SXRD Digital Signal Driver

CXD3554GG

1. Description

The CXD3554GG is a signal processor + digital signal driver for single panel SXRD. This chip supports frame sequential drive, and integrates panel correction functions such as gamma correction and color shading correction, and projector signal processing such as keystone (geometric) correction and edge blending correction onto a single IC. An on-chip DRAM supports frame sequential drive. Vertical only keystone (V keystone) correction can be realized using only the on-chip SRAM and connection of an external DDR2 enables horizontal and vertical keystone (geometric) correction. MIPI® interface input and mini-DSI interface output is supported. This IC supports driving of Sony LCD panels such as WXGA and the Full HD standard.
(Application: LCD projectors and other video equipment)

2. Features

- Drives various single panel SXRD panels such as WXGA and Full HD
- Various on-chip picture quality adjustment functions such as white balance adjustment and gamma correction
- MIPI® interface input supports D-PHY v1.1 and DSI v1.1
- mini-DSI output supports 800 Mbps
- On-chip DRAM for frame sequential drive
- Supports external DDR2 SDRAM (when using horizontal and vertical keystone geometric correction)
- Supports I2C and 3-wire serial communication
- Able to control various ICs as the I2C master
- Generates light source (LED, laser, etc.) control signals

3. Package

LFBGA 289pin 12mm PKG 0.65mm Pitch

4. Structure

Silicon gate CMOS IC

MIPI® is a registered trademark of MIPI Alliance, Inc.
5. Operating Conditions

- **Supply voltage**
  
<table>
<thead>
<tr>
<th>Voltage Source</th>
<th>Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCK12, AVDD12_Osc, AVDD12_RMIPI, AVDD12_LMIPI, VDDIPHY, VDD2, VDDQ12, VDDCA12, AVDD12_DSI, VCCK12_MINI, AVDD12_PLLM1, AVDD12_PLLM2, AVDD12_PLLPIX, AVDD12_PLLFS</td>
<td>1.18~1.30 V</td>
</tr>
<tr>
<td>AVDD18_RMIPI, AVDD18_LMIPI, VDDE18_CK, VDDE18, VDD18_LPDDR2, AVDD18_DSI, AVDD18_PLLM1, AVDD18_PLLM2, AVDD18_PLLPIX, AVDD18_PLLFS</td>
<td>1.70~1.90 V</td>
</tr>
<tr>
<td>VDD33_IO, VCCIO_PLL1, VCCIO_PLL2</td>
<td>2.97~3.63 V</td>
</tr>
</tbody>
</table>

- **Operating temperature**
  
<table>
<thead>
<tr>
<th>Temperature Source</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topr</td>
<td>-25~+75 °C</td>
</tr>
</tbody>
</table>

- **Thermal resistance**
  
<table>
<thead>
<tr>
<th>Thermal Resistance</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>θja (condition: air flow 2m/s)</td>
<td>16.8 °C/W</td>
</tr>
<tr>
<td>Ψit</td>
<td>0.29 °C/W</td>
</tr>
</tbody>
</table>

6. Operation Frequency

- **Video I/F**
  
<table>
<thead>
<tr>
<th>Interface</th>
<th>bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIPI® RX</td>
<td>80~1500 Mbps</td>
</tr>
<tr>
<td>mini-DSI TX</td>
<td>200~800 Mbps</td>
</tr>
</tbody>
</table>

- **Core**
  
<table>
<thead>
<tr>
<th>Block</th>
<th>Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre block</td>
<td>70~312 MHz</td>
</tr>
<tr>
<td>Main1 block</td>
<td>35~156 MHz</td>
</tr>
<tr>
<td>Main2 block</td>
<td>35~156 MHz</td>
</tr>
<tr>
<td>Post block</td>
<td>25~100 MHz</td>
</tr>
</tbody>
</table>

- **Input CLK**
  
<table>
<thead>
<tr>
<th>CLK Source</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTALIN</td>
<td>24.576, 33, 48 MHz</td>
</tr>
</tbody>
</table>
7. Block diagram

CXD3554GG

- MIPI® D-PHY Rx
  - Pre Image Processing
    - Sharpness
    - Color
    - Gamut
    - Edge
    - Blending
    - KeyStone
    - Gamma
    - Uniformity Correction

- Frame Rate Converter (color sequential)
- Frame Memory
- Post Image Processing
  - Vcrosstalk Correction

- mini-DSI Tx

- Clock control
- HOST I/F
- Memory Control
- DDR2: When using the keystone function

- MIPI® D-PHY 4lane x 2port
- 3.3V
- 1.8V
- 1.25V

- X’tal
- I2C
- SPI

- Timing Signals
- mini-DSI

- DDR2

- TG
- I2CM
Product Summary

Digital Signal Driver/Timing Generator

CXD3556GG

1. Description

The CXD3556GG incorporates digital signal processor type RGB driver, timing generator functions, panel correction functions such as gamma (panel gamma) and color shading corrections, and projector signal processing such as keystone (geometric)/distortion correction and pseudo 4K function onto a single IC. The input supports LVDS, V-by-One® HS and MIPI® I/F, and the output supports V-by-One® HS and MIPI® I/F.

The CXD3556GG can output timing signals for driving various Sony LCD panels from XGA to WUXGA standards and also support a wide range of resolutions such as WQXGA, 4K2K, and 4K2.4K standards.

(Aplications: LCD projectors and other video equipments)

2. Features

- LVDS RX I/F (for input) supports up to 1.05Gbps
- V-by-One® HS RX I/F (for input) supports up to 4Gbps
- MIPI® RX I/F (for input) supports up to 1.5Gbps
- V-by-One® HS TX I/F (for output) supports 4Gbps
- MIPI® TX I/F (for output) supports up to 1.5Gbps
- MIPI® RX and TX I/F supports D-PHY v1.1 and DSI v1.2
- Integrated VESA DSC (Display Stream Compression) Encoder and Decoder v1.2a (12bpp and 8bpp compression modes) onto MIPI® RX and TX
- Supports I2C bus and 3-wire serial communication
- Controls various ICs as the I2C master
- Drives various Sony projector LCD panels such as XGA, WXGA and WUXGA
- Supports various resolution standards such as WQXGA, 4K2K, 4K2.4K
- Supports PU ARM926EJS (4K I-cache / 4K D-cache, JTAG ICE interface and Watchdog timer)

3. Package

625pn FCBGA 21mm □ PKG 0.8mm Ball Pitch

4. Structure

Silicon gate CMOS IC

\*V-by-One® is a registered trademark of THine Electronics Corporation.
\*MIPI® is a registered trademark of MIPI Alliance, Inc.
\*ARM is a registered trademark of ARM Limited.
## 5. Operating Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>AVDD08_VBO_TX, AVDD08_VBO_RX1, AVDD08_VBO_RX2, AVDD08_PLL1, AVDD08_PLL2, AVDD08_PLL3, AVDD08_PLL4, VDD, AVDD08_MIPI_TX_PLL</td>
<td>0.72</td>
<td>0.8</td>
<td>0.88*</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>AVDD12_MIPI_TX1, AVDD12_MIPI_TX1, AVDD12_MIPI_TX2, AVDD12_MIPI_TX3, AVDD12_MIPI_TX4</td>
<td>1.14</td>
<td>1.2</td>
<td>1.26</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>AVDD18_VBO_TX, AVDD18_VBO_TX_PLL, AVDD18_VBO_RX1, AVDD18_VBO_RX2, AVDD18_LVDS_RX0, AVDD18_LVDS_RX1, AVDD18_LVDS_RX2, AVDD18_LVDS_RX3, AVDD18_LVDS_BUF0, AVDD18_LVDS_BUF1, AVDD18_LVDS_BUF2, AVDD18_LVDS_BUF3, AVDD18_PLL1, AVDD18_MIPI_TX, AVDD18_MIPI_TX_PLL, AVDD18_MIPI_RX</td>
<td>1.62</td>
<td>1.8</td>
<td>1.98</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VDD33_GPIO</td>
<td>2.97</td>
<td>3.3</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>Topr</td>
<td>-20</td>
<td>-</td>
<td>75</td>
<td>Degree C</td>
</tr>
</tbody>
</table>

*In case of the maximum power consumption under high load use case, use this IC with 0.8V power system lowering by the maximum range to 0.8V so that power consumption (Po) is allowable dissipation (Pd) or less.

## 6. Operation Frequency

- **Video I/F**
  - LVDS RX: 175 ~ 1050 Mbps
  - V-by-One® HS RX: 0.6 ~ 4.0 Gbps
  - MIPI® RX: 0.133 ~ 1.5 Gbps
  - V-by-One® HS TX: 0.6 ~ 4.0 Gbps
  - MIPI® TX: 0.133 ~ 1.5 Gbps

- **Input CLK**
  - XTALIN: 25±1.5%, 33±1.5% MHz

- **Output CLK**
  - PCLK: 6 ~ 37.5 MHz
8. Package Outline

(Unit: mm)

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**SONY CODE**: FBGA-625P-691

**JEITA CODE**: P-FBGA625-21x21-0.8

**JEDEC CODE**: ---

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**PACKAGE MATERIAL**: Sn-3.0Ag-0.5Cu-0.05Ni

**ORGANIC SUBSTRATE**: ---

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**PART NO.**: AP-2000-625GGBR1

**REV.**: 0

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**ISSUED**: 20.04.16

**REVISED**: ---

**PRODUCTION LINE**: COMPLING DIV.

**REMARKS**: SONY SEMICONDUCTOR MANUFACTURING

**PKG CODE**: GG-625-AWBR

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